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AUSTIN SILICON INCORPORATED
www.austinsilicon.com
Company Resume

Austin

OBJECTIVE:

To provide quality short and long term consulting services for the following VLSI related projects:

Circuit Design:
- Full Custom Circuit Design For Digital and Mixed Signal Platforms
- Design, Development and Testing Of Low Power and High Power IO, Padring and ESD circuits
- Library Development, including layout supervision
- Testing, Migration and Characterization of Existing Designs
- New Process Evaluation
- Full Project Management
- Training – Design, Simulation and Debug

Logic Design, Test and Related Engineering Development:
- Logic Synthesis For Control Units Using Cadence-Synopsis and Other Packages
- Custom Logic For ALU, MMU and Others
- Verilog, VHDL and Other Simulation Tools
- Overall Project Management
- Impart Training To Individuals

Layout Design, Place and Route, Floor Planning:
- Custom, Synthesized and Migrated platforms Design
- Training – Instruction, Monitoring and Review

EXPERIENCE AND TRAINING:

We at AUSTIN SILICON, INC. take great pride in the employees we send to the customer job site to represent our company. Each engineer brings with him many years of industry experience and familiarity with the latest tools. Training on circuits and other aspects of design are imparted by qualified engineers on a need basis.

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CLIENT HISTORY (Example):

Coinlab November 2012 through April 2013
Scientific devices company. They are headquartered in Seattle.

Services Provided:

- Designed padring, clock module, and datapath design

Intrinsity Incorporated January 2007 through February 2008
Intrinsity is known for its unique FAST14 solution to high speed integrated solutions. They are headquartered in Austin.

Services Provided:

• Designed a Jtag TAP controller with interfaces for 2.5 Ghz Memory Bist and OnChipDebug. Delivered verilog RTL, synthesis deck, complete floorplan in 90nm with power grid, and Pathmill analysis. The Magma Blastfusion tools were used for all deliverables.

• Designed 2GHz 64 bit Timer, 32 bit Decrementer and Timebase unit in TSMC 90nM process. Delivered RTL, STA and Floorplan.
• Developed synthesis ready 2.5 Ghz custom cell library (Magma Volcano) for 65Nm TSMC process.
• General stdcell library support for various technologies.

Intel (Chandler) 2006
Intel is the pre-eminent chipmaker in the world and does not need an introduction.

Services Provided:

• Migrated the Xscale core named Manzano from 130nm to 65nm which included the following work:
• Circuit fixes related to signal edge rates, speed paths, signal integrity.
• Logic equivalency tests using LEC and architectural verification runs using Intel's own pattern matching tools.
• Pathmill timing analysis tool was used to analyze and fix problems with domino and other non-standard designs.
• Layout changes were verified both visually and using erc and lvs.
• All tasks were completed and delivered in a timely manner.

Coherent Logix 2005 through 2006 – Circuits and Verification
Coherent Logix is a small company in Austin. They do defense related designs and their principal customer is the DoD.

Services Provided:

• Full chip schematic timing analysis, synthesis methodology, IO/ESD designs, Power Management architecture and C4 bumps based Padring layout supervision of the HyperX processor. This is a large network based arrayed processor containing 15M transistors meant for Hyper Spectral applications.
• Full chip timing analysis on an extracted netlist customized for this purpose. The analysis was carried out using Cadence's RC and FE (First Encounter) tools.
• Developed RC synthesis scripts for the team. The script has been successfully used to synthesize varied designs within the chip and uses methods to ensure proper interface timing between the arrayed processors. Both Synopsis and Cadence's tools can use the scripts.
• Assisted with full chip gate simulation efforts using Modelsim and Debussy.
• Designed a 1.8v EIA-644 LVDS IO driver and differential receiver with a low power shutdown mode. The receiver has 100mv sensitivity over the entire 1.8v range. This is a part of a complex IO cell that can switch from being an LVDS cell to SSTL, LVTTL or GPIO just by flipping some bits. The ESD design is based on IBM's RC clamps and diode models available for the CMOS8RF 130nm process. The Padring is capable of being switched off in sections with an external or software Wakeup feature. Designed the driver for the 1.8v SSTL_18 outputs.

Advanced Micro Devices 2003-2004, 2012
AMD is a well-known desktop chipmaker with popular products such as Athlon and the K5 processors. We consulted with the Opteron design team in Boston and Austin to help develop the latest pcix2 specification hyper transport IO for production. This is the version 2.0 of the pcix specification intended to run at 533 mbit data rate. Initial tests reveal that the part is functional at 533 mbit/s, this the first time this performance has been achieved in the industry.

Services provided:

• Provided backend support namely timing driven place and route, clock tree synthesis, primetime analysis and custom library cell development for high speed clocks.
• Tested the design for 133, 266 and 533 Mbit/s compliance and wrote a report. The job was to help with design and debug of the IO cell and testing the output buffer and input buffer for spec compliance. Other efforts were applied in evaluating the package limitation at 533 mbits and identifying high current modes during sleep state.

• Delivered .LIB timing files. The job included writing the .lib files for global timing and place and route tools. Hspice analysis of arc's relating to core-to-core and core-to-pad signals were determined.

MathStar Corporation 2002 through 2003
Mathstar Corp. is based in Minneapolis, Minn. They are an up-and-coming company breaking ground with their proprietary FPOA's (Field Programmable Object Arrays) and DSP parts designed in 130nm TSMC process. We consulted for MathStar via a contract through North Shore Circuit Design based in Austin, TX.

Services Provided:

• The job was to design a unique 1Ghz Field Programmable Object Array that was hexagonal in shape to allow a 6-way communication between independent processor/neighbors. The part had networking application and following work was done during the design phase:
• Modeling of the architecture to confirm 1Ghz speed. This included modeling the critical datapath to latch and forwarding to the worst-case neighbor within a specified amount of time.
• Designed and tested library components for 1GHz operation. This included designing the cells, writing verilog description and testing gate and behavioral models.
• Clock design and routing for the whole chip.
• Layout of the interconnected processors floor plan, Metal Plan and Chip Plan.

Silicon Metrics Corporation (Magma Design) 2002
Silicon Metrics now Magma Design is a well-known EDA company known for the groundbreaking SiliconSmart ™ Tools including CellRater, MemRater and IORater. Their clients include Intel, AMD and other well-known chip companies. We helped design their flagship product the IORater. This product allows a company to characterize any kind of IO cell with canned or custom IO specs. The product is capable of compliance testing LVDS, USB1.0, USB1.1, I^2C, I^2S, SDRAM Interface, and other designs. The products has had good reviews and made the cover of Electronic Design Magazine in August 2002.

Austin Silicon Incorporated directed and/or developed almost all aspects of the IORater product.

• Product Definition and Architecture for the IORater: This included defining the tool suite for licensing purposes. The functional architecture of the product that defined in detail how various components of the product would interface with each other. For example it indicated how many different types of input, scratch and output files would be needed for each published specification. And how the tool would decipher each specification.
• Details of the spice stimuli needed for each specification and circuit modeling of the harness needed to model the chip external and Internal worlds. The harness for example represents resistors tied to supplies for IOH and IOL current tests.
• Specifics of signal measurements needed to verify compliance to the specifications.
• Presentation of the compliance and error reports with graphical display of the failures.
• Help with technical publications.
• Identification of target group for marketing purposes.
• Customer visits, and EIA certification.

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Education:

MSEE, University Of Texas At Austin
MSc. Atomic And Molecular Physics, University Of Karachi
BSc. Physics, University Of Karachi

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