607 Bandera Drive, Allen, TX 75013
(512) 323-5518 Cell / (972) 559-8402 Land Line
zahid@austinsilicon.com

Zahid Ahsanullah

Objective

EMIR powergrid rail integrity engineer experienced in 16nm+ finfet and older Planer technologies. Expert level author of application notes and rapid adoption kits. Expert in Voltus, VoltusFi, Spectre AMS. AMS-XL, Virtuoso tools, low power CPF, UPF technologies, ESD planning and more. Comfortable with digital, analog, mixed signal, AoT and DoT designs.

Profile

Application Engineer supporting Voltus Rail Analysis tool on CPF, UPF based design on 16nm process. Expert in VoltusFi transisitor level powergrid views (PGV) for analog macros. Previously an application engineer supporting frontend-backend and conformal tools. Worked on rtl-gds flow on Intel's one teraflop Knight's Corner (KNC) processor and the Haswell processor. Circuit engineer on intel's 8 Ghz Tejas chip and low power DSP chips. Patents on Mixed Signal IO circuits.

Core competencies include: Voltus Power Integrity, VoltusFi transistor level macro modeler for AoT designs, RTL Compiler (RC), floor-planning, timing driven Place and Route (PR/PNR), clock tree synthesis (CTS), clock mesh design (CTM), Design compiler (DCT), Physical compiler (ICC), Conformal tools Verplex/LEC Logical Equivalency Checker, Primetime (PT/STA), Cadence Power Format (CPF), Universal Power Format (UPF IEEE 1801). Array circuits Spice modelling, library cell development, custom asic, IO circuits (usb, i2c, ddr, lvds, sstl, lvttl), Pathmill, Jtag design, LVS, ERC, DRC, electromigration/IR drop (EM/IR), Signal Integrity (SI), layout extraction, Modelsim, Debussy, Hspice, Spectre.

Professional Experience

(2013-Present) (Cadence Design Systems. Austin, TX)

Lead Application Engineer

- Voltus and VoltusFi support for 7 leading edge customers. Previously supported Synthesis (RC Compiler), Formal Equivalence (Verplex/LEC), Conformal Low Power (CLP), Common Power Format (CPF), IEEE 1801 UPF. Support for 28nm-16nm design. Also supports 130nm and older technologies. Author of several Application notes including Electromigration, ESD and CPF. Expert in Rapid Adoption Kits design and customer testcase development.

(2012-2013) (Consultant. Austin, TX)

Design Engineering Consultant

- ***Coinlab Inc., Seattle, WA (2013-)***: Completed IO and Padring circuit design for 2Ghz data transfer in 65nm SMIC process. Worked on physical synthesis of core and laid down the groundwork for floorplanning and Placement using Silvaco backend tool suite.

- ***Advanced Micro Devices, Austin, TX (2012-2012)***: Integration of Kryptos testchip. Work included PNR, clock-tree synthesis, floor-planning, STA of lib cells and io signals, EM/IR analysis and custom clock macros development.

(2008-2012) (Intel Corporation. Hillsboro, OR)

Analog Integration Engineer: Many Integrated Core(MIC) Design, Digital Enterprise Group (DEG)

- Worked on low power version of the Haswell (HSW) processor designed for throughput computing. Recently completed design of the 1 terraflop Knights Corner (KNC) processor. KNC is the newly released 50+ core processor based on the new 22nm 1.6 Ghz Tri-Gate (Finfet) process. This process is characterized by low leakage at low Vt and high voltage. It has a phenomenal high frequency performance at low voltage. HSW uses a low voltage/power version of this process meant for next version of Macbook Air with 16 hours battery time.
- HSW -- Worked on 3 latch/flop based synthesis blocks. Responsible for frontend and backend timing/critical-paths/CTM/power/DFM design. LEC and fullchip timing fixes. Provided solution from DCT to metal fill.
- KNC -- Completed backend integration (floor-planning to metal fill) of 3 top level analog/digital *Megablocks* namely *LDIO, LDIOPLL and LPCPLL*. The first is an IO block and the others are analog PLL's. Managed block/chip level static timing analysis (STA) using Synopsis DC and ICC tools. Used frontend/physical Universal Power Format (UPF) based synthesis to do signal and power floor-planning of 5 local and top level supplies. Completed CTS of 1.6 Ghz core clock and 100 Mhz test clocks routes. Manually pre-routed critical clocks. Completed LEC and fullchip noise analysis.
- UPF Low Power Design -- Pioneered Synopsis's Power Aware UPF and Powerintent based tools to place and route an IO and PLL blocks with embedded regulators. This allowed RTL to be free of all power definitions. It also eliminated manual level-shifter insertion between power domains by auto placing them. Five power domains including regulated and switched ones were automatically floor-planned by this method.

(2001-2008) (Consultant. Austin, TX)

Design Engineering Consultant

- ***Intrinsity Incorporated. Austin, TX (2007-2008)***: Designed a TSMC 90nm Jtag TAP Controller, MBIST Jtag interface, On Chip Debug (ocd) Jtag 2.5 Ghz interface, 2 GHz 64 bit timer, 32 bit Decrementer and Timebase unit. Delivered RTL, Synthesis, Floorplan, and Pathmill timing analysis. Used Magma BlastFusion tools.
- Created 2.5 Ghz standard cell library Volcanos using Magma. These components were designed with custom cells that replaced slow blocks in the ARM core. Completed power domain analysis of the revised ARM core.
- ***Intel Corporation. Chandler, AZ (2006-2006)***: Migrated the Xscale core Manzano from 130nm to 65nm. Fixed edge rates, speed paths, SI, LEC, architectural verification using Intel's pattern matching tools. Pathmill timing analysis of domino designs. Completed ERC and LVS.
- ***Coherent Logix. Austin, TX (2005-2006)***: Completed full chip timing analysis, gate sim, synthesis setup, area array C4 IO/ESD designs, power management unit and padring of the HyperX processor. This is an arrayed processor containing 15M transistors meant for Hyper Spectral applications. Tools used were Cadence RC, FE, Modelsim and Debussy.
- Designed a 1.8v EIA-644 LVDS IO driver and differential receiver with a low power shutdown mode. The receiver has 100mv sensitivity over the entire 1.8v CMR. This is a part of a complex IO cell that can switch from being an LVDS cell to SSTL, LVTTL or GPIO just by flipping some bits. The ESD design is based on IBM's RC clamps and diode models available for the CMOS8RF 130nm process. The Padring is capable of being switched off in sections with an external or software Wakeup feature. Designed the pad driver for the 1.8v SSTL_18 outputs.
- ***Advanced Micro Devices. Austin, TX (2004-2004)***: Designed a pcix2.0 533 mbits/s IO. This IO is one of a kind and handles all pcix specs namely 33, 66, 133, 266 and 533 mbits/s. PrimeTime, Starsim simulations of all 64 IO bits. Delivered Technical Analysis Report. Part is used in Opteron interfaced to a hyper transport bus.
- Designed the above cell using proprietary slew rate control using 130nm UMC process with 1.2V supply for core and 3.3V and 1.5V for the output buffers (mode 1 and 2 respectively). This is a non-analog design so it is easily scalable.
- **Patent** (in progress): Process Switchable Low Noise Output Buffer.
- ***Mathstar Incorporated. Dallas, TX (2003-2003)***: Designed clock-tree, speed-path circuits and library cells for a 1Ghz networking chip called the Field Programmable Object Array Processor. Design uses hex shaped processors array for 6-way communication.
- ***Silicon Metrics/Magma Design. Austin, TX (2002-2002)***: Designed the EDA tool SiliconSmartIO. This was a flagship product used to certify and design specialized as well as standard IO's. The tool also does Padring analysis and offers insight into design flaws. The capability includes compliance testing LVDS, USB, I2C, I2S and SDRAM Interface by using Spice analysis customized for each specification. The product was on the cover of Electronic Design. Deliverables included: a) A textual description of modeling issues implied by the specs b) Spice decks for each model c) Methods of signal measurements to verify compliance to published specs d) Interface to the EDA tool SiliconSmart Cellrator used to generate static timing files and .LIB e) Graphical display of compliance f) Help with technical publications and press release g) Product licensing, h) Customer support, and EIA certification.

(1998-2001) (Intel Corporation. Austin, TX)

Design Engineer: StrongArm, Xscale, Tejas Desktop Platform Group (DPG)

- Developed 7GHz library cells in 2 aspect ratios for DPG's 64bit processor Tejas. Completed Low Noise 50ps CK-Q FF, CSA, Fast 72 bit adders, 30ps Zero Detects. Delivered Verilog model, Static Timing analysis, .LIB, Noise Analysis tests.
- Floor-planned the ARM Core and power management module. Designed ESD, Padring, USB and a Low Noise Programmable IO buffer for the low power 600 MHz, 0.25W Xscale part called Cotulla. Created Pad-Package mapping, designed Package Substrate, Package Pinorder, tests for 0.25W operation and tests for 75uA Sleep and Drowsy Modes. These modes along with Power Island circuits were innovations for low power. Verified design by modeling and simulating 256 pad cells in VHDL, wrote test fixture for the Padring, hand created .LIB files for IO Cells including analog ones, ran STA on extracted Padring. Created IBIS models for the drivers as well as board models for various applications.
- Designed the SDRAM memory interface IO buffers for the low power 0.5 Watt StrongArm SA1110. The design incorporates a Sleep Mode that switches off some supplies to core and Padring under Powersave conditions. Wrote Verilog models for the IO cells and Jtag and ran Regression tests. Developed and modeled design rules for boards and created IBIS models. Attended training for Synopsis Black-Box Timing Model.
- **Patents**: A Low Leakage Level Translator, USB Cable Disconnect Detect, Driver Z-Match output buffer, Regulator Independent IO Sleep Controller.
- **Award:** Leaping Lizard Award For Excellent Contribution.

Previous Tenures: Motorola Incorporated. **Defensive Publication:** Preventing False Latching In VLSI Circuits.
Advanced Micro Devices. **Patent Accepted:** A Supply Bounce Controlled Output Buffer.

Education

MSEE	University Of Texas at Austin	Austin, TX
MSc (Atomic and Molecular Physics)	University Of Karachi	Karachi, Pakistan
BSc (Physics)	University Of Karachi	Karachi, Pakistan

Interests

Power Aware methods (UPF) and Low Power design

TOP